AMENDMENTS TO THE CLAIMS

Kindly amend the claims as follows

1. (Cancelled)

2. (Currently amended) An integrated circuit design kit comprising:
means for generating one or more circuit components topologies; and
means for designing one or more critical interconnect lines topologies.

3. (Original) The kit of claim 2 wherein said interconnect line topologies are predefined.

4. (Currently amended) The kit of claim 2 and further comprising one or more circuit components models.

5. (Currently amended) The kit of claim 2 and further comprising one or more critical interconnect lines models.

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6. (Currently amended) A design topology of critical interconnect lines.

7. (Currently amended) The design topology of claim 6 wherein said topology is predefined.

8. (Currently amended) The design topology of claim 6 comprising a definite current return path.

9. (Currently amended) The design topology of claim 6 wherein said design topology comprises ~~is supplemented by~~ a model describing ~~comprising~~ one or more of said following electrical parameters: capacitance, low frequency inductance, high frequency inductance, low frequency series resistance, high frequency series resistance, TEM impedance, and matrix representations of one or more of said parameters.

10. (Cancelled)

11. (Currently amended) The design topology of claim 6 wherein said topology comprises one or more signal wires and one or more shielding wires.

12. (Currently amended) The design topology of claim 11 wherein said one or more shielding wires is one or more side shielding wires located on one or more sides of said signal wires.

13. (Currently amended) The design topology of claim 11 and wherein said one or more shielding wires is a bottom shielding wire.

14. (Currently amended) The design topology of claim 11 and wherein said one or more shielding wires is one or more shielding layers.

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15. (Currently amended) A computer software product for designing an integrated circuit, said product comprising a computer readable medium in which program instructions are stored, which ~~instructions,~~ when read by a computer, cause said computer to create a design topology of critical interconnect lines.

16. (Currently amended) The product of claim 15 and further comprising instructions, which ~~instructions,~~ when read by a computer, cause said computer to create a design model of critical interconnect lines.

17. (Currently amended) A computer software circuit design product for designing an integrated circuit, said product comprising a computer readable medium in which program instructions are stored, which ~~instructions,~~ when read by a computer, cause said computer to deploy ~~create a~~ said circuit design product ~~kit,~~ said circuit design product comprising ~~a~~ means for designing topology of critical interconnect lines.

18. (Currently amended) The product of claim 17 and further comprising instructions, which ~~instructions,~~ when read by a computer, cause said computer to create a design model of critical interconnect lines.

19. (Cancelled)

20. (Cancelled).

21. (Cancelled)

22. (Currently amended) The method of claim ~~19~~ 32, wherein said integrated circuits are analog and mixed signal (AMS) circuits or application specific integrated circuits (ASIC).

23. (Currently amended) The method of claim ~~19~~ 32, wherein in (b), the step of defining comprises choosing from a set of predefined parameterized design topologies.

24. (Currently amended) The method of claim ~~19~~ 32, wherein in (b), the step of defining comprises defining a set of design topologies.

A' cont'd

25. (Currently amended) The method according to claim ~~19~~ 32, wherein said schematic design comprises models of said one or more transmission line topologies.

26. (Original) The method according to claim 25, and further comprising the step of calculating one or more electrical parameters of said models.

27. (Original) The method according to claim 26, wherein said one or more electrical parameters includes one or more of the following: capacitance, low frequency inductance, high frequency inductance, low frequency series resistance, high frequency series resistance, TEM impedance, and matrix representations of one or more of said parameters.

28. (Currently amended) The method according to claim ~~19~~ 32, wherein step (b) comprises:

using one or more of said following to identify said critical interconnect lines: estimated length, metal level assignment, signal integrity, timing requirements and manual user selection.

29. (Currently amended) The method according to claim ~~19~~ 25, and further comprising creating parameterized cells from said models.

30. (Original) A method for designing integrated circuits wherein defining said chip architecture and a floor plan comprises defining critical interconnect wires.

31. (New) A system for integrated circuit design comprising:

means for designing a high level circuit design, said high level circuit design including a chip architecture and a floor plan, whereby major design blocks and their locations are defined, and further including one or more critical interconnect wire topologies;

means for designing a schematic design at least including one or more circuit components and one or more critical interconnect wire models; and

means for designing a physical layout at least said one or more circuit components and said one or more critical interconnect wire topologies.

A' cont'd

32. (New) A method for designing integrated circuits (IC), said method comprising the steps of:

(a) defining a chip architecture and a floor plan;

(b) identifying one or more critical interconnect lines, and defining one or more transmission line topologies for design of said critical interconnect lines;

(c) determining a schematic design of said IC from said chip architecture floor plan and said critical interconnect line topologies; and

(d) defining a physical layout of said IC at least from said chip architecture floor plan and said critical interconnect line topologies.

33. (New) The method according to claim ~~19~~ 32, wherein said physical design comprises parameterized cells of said one or more transmission line topologies.

34. (New) A system for integrated circuit design comprising:

means for designing a schematic design at least including one or more circuit components and one or more critical interconnect wire models, wherein said one or more critical interconnect wire models are parameterized cells of one or more transmission line topologies.

35. (New) A system for integrated circuit design comprising:

means for designing a schematic design; and

means for designing a physical layout including at least one or more circuit components and one or more critical interconnect wire topologies, wherein said one or more critical interconnect wire topologies are parameterized cells of transmission lines.

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